

IC Package innovations

New IC package begs the question 'Does a well designed package need a socket?'

Over the last decade and a half there has been a major shift in electronic packing technology away from peripherally leaded through-hole and surface mounted components to area array packages such as the BGA. Over that same time period there has been a nearly simultaneous trend to reduce the size of these packages. This is because one of the intrinsic advantages of area array packaging and interconnection is that it allows the user to package and assemble high pin count devices in the most compact form and do so at assembly high yield. While yields may be high for solder joints, it is moot if the package is not operational. Thus, through most of the history electronics industry (at least over the last few decades), virtually every integrated circuit package manufactured has required at least one electrical test step on their way into an electronic product. The reason for electrical test, as alluded to above, is obvious: the risk of wasting time making a product with devices that are 'dead on arrival' is one that is well worth avoiding. This is especially true when the rework process can degrade the quality of the substrate and nearby devices. Moreover, with the mandate for lead-free solders being leveled on the industry by the European Union on 1 July 2006, rework risk is only going to get worse because most of the lead-free solders chosen to replace traditional solders melt at temperatures 30°C - 40°C higher than eutectic tin-lead solder.

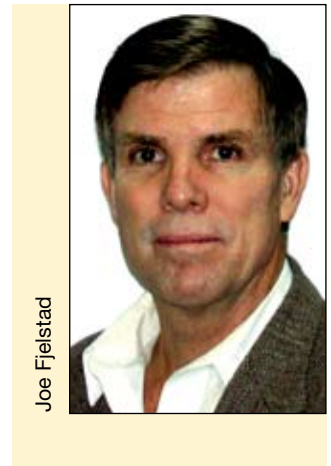
Thus there are some clearly compelling reasons to perform test. However, in accepting the need for test, one also

accepts the price that must be paid to acquire test equipment and test sockets. These can be pricey adders to the cost of package assembly. For example, while the cost of test may be low for simple devices, with increases in complexity and pin count there is also an increase in the cost of testing and test hardware. Standards for package pin out help to ameliorate some of the cost of test by presenting the opportunity to use a common test bed for a number of prospectively different parts, but they do not eliminate the cost. In addition, there is an element of maintenance associated with the socket that makes it necessary to clean the contacts from time to time to remove metal debris and oxides and thus assure a good electrical test. But what if no socket was required?

This is a question that a team of research and development engineers at chip scale packaging pioneer Tessera, lead by Tessera Fellow Dr. Belgacem Haba, asked themselves. The results of their investigations were presented at the Burn in and Test Socket Workshop held in Phoenix, AZ in March of this year. Those results are most interesting. What Dr. Haba and his team did was, in essence, make the terminations on the package serve as the resilient contacts for electrical test. There have been some analogous attempts in the past using other methods, the most notable being micro springs, such as was described by Formfactor, Inc.; however, that company abandoned the attempt when they saw that the solution they developed was well suited to probe card contact applications.

In contrast, the Tessera solution, as disclosed, is one that it appears will be able to deliver on the both the cost and the performance promises that a compliant pin contact technology offers. As can be seen in *Figure 1*, the package contacts are actually microscopic posts of extremely uniform height. Since the posts are substantially made of etched copper, they are not going to easily deform or smear as do solder balls. The result is a robust contact that obviates user concerns over non planarity. Moreover, it makes it possible to make contact with planar lands on the test bed. The presentation materials indicate that it is possible to make contact on such surfaces using relatively low gram load forces and with no appreciable damage to either of the contact surfaces. One of the keys to making it all work is Tessera's patented compliant layer that resided between the contacts and the die.

In summary, a new IC packaging structure in being



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introduced that appears to be capable of either obviating or greatly simplifying test sockets for IC packages and while the development work was focused on chip scale packages, it is a concept that could well offer benefit to packages having greater pin counts and larger size. Dr.Haba's presentation from the conference can be found at: <http://www.tessera.com/spotlight.htm>

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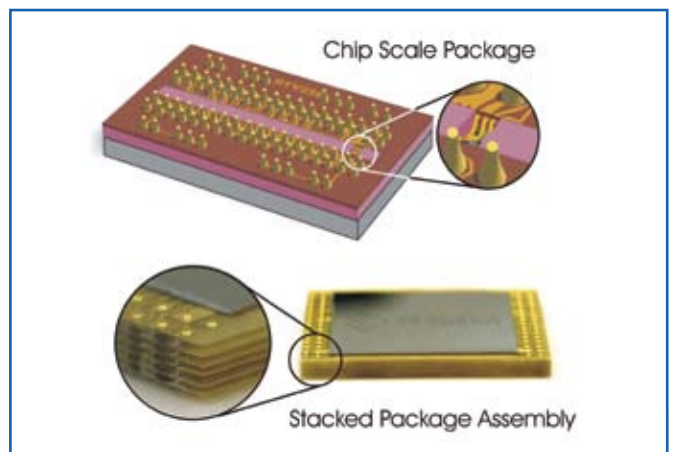


Figure 1. Examples of the micro pin contact structures. The pins are highly planar but also offer some compliance and make contact at low gram force. The photos are of actual packages is stacked format, one of the other benefits the package offers when pins are deployed to the periphery. The six high stack is under 1mm in height.